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EXAMINER	
KE, PENG	

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN W. ROGERS
and JASON S. KING

Appeal 2008-005684
Application 09/742,946
Technology Center 2100

Before JAMES D. THOMAS, HOWARD B. BLANKENSHIP, and JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-52, which are all the claims in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Representative Claims

1. A method for propagating type information for hardware device nodes in a graphical program, wherein the method operates in a computer including a display screen and a user input device, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program;

associating the first hardware device node with a hardware device;

displaying on the display screen a second hardware device node in the graphical program in response to user input;

connecting the first hardware device node to the second hardware device node in response to user input;

propagating information from the first hardware device node to the second hardware device node, wherein the information specifies the hardware device with which the first hardware device node is associated, wherein said propagating occurs in response to said connecting the first hardware device node to the second hardware device node;

wherein the graphical program is executable by the computer.

10. A method for performing type checking for a hardware device node in a graphical program, wherein the method operates in a computer including a display screen, the method comprising:

displaying on the display screen of the computer a first hardware device node in the graphical program in response to user input, wherein the graphical program comprises a plurality of interconnected nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the graphical program;

associating the first hardware device node with a first hardware device class in response to user input;

selecting a method or property of the first hardware device class for the first hardware device node in response to user input;

changing the first hardware device node to have an association with a second hardware device class in response to user input; and

performing type checking to determine whether the method or property is valid for the second hardware device class, in response to said changing the first hardware device node to have an association with the second hardware device class;

wherein the graphical program is executable by the computer.

Examiner's Rejections

Claims 1-14, 16-29, and 31-52 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Teranishi (US 6,117,183).

Claims 15 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Teranishi and McKaskle (US 5,481,741).

DISCUSSION

Section 102 - Claims 1-9, 18-25, 32-38, 43, 44, 47, 48, 51, 52

The Examiner finds that Teranishi describes, in text at column 7, displaying a first and a second hardware device node as recited in instant claim 1. Column 7 of the reference refers to Figure 7, which depicts a display screen of a CAD apparatus for placement of components in a logic circuit (e.g., placement on a printed circuit board).

Appellants argue that Teranishi does not disclose propagating information from the first hardware device node to the second hardware device node, wherein the information specifies the hardware device with which the first hardware device node is associated.[2] The Examiner's statement of the rejection refers to column 4, lines 5 through 26 of Teranishi for the disclosed feature. That portion of the reference describes constructing error path lists (EPLs) that indicate where problematic time delays may exist as a result of component placement (*e.g.*, Fig. 2, "ERROR PATH LIST" in window 2).

[2] Although claim 1 might appear to recite "propagating" information from one icon to another on a display, the "nodes" are underlying data structures between which data is transferred. *See, e.g.*, Spec. 29:24 - 33:21.

The Examiner responds to Appellants' above-noted argument in the Answer.

> In this case, Teranishi teaches propagating information from a first hardware device node to a second hardware device node of a graphical program because Teranishi's CAD program passes position data of first hardware device node to the second hardware device in order to calculate the delay time between the two device node. (see Teranishi col. 8, lines 10-55)[.]

Ans. 15.

However, we do not find any disclosure in the indicated sections of the reference with respect to information transfer from one component (node) to another. Rather, in our reading of the reference, software programming calculates the data delay values for paths between any of the components. We further do not find any disclosure (or need) of passing position data of a first hardware device node to a second hardware device in order to calculate the delay time between the two device nodes, as alleged by the rejection.

Independent claims 18 and 32 are rejected on the same basis as claim 1 but recite similar limitations for which the rejection of claim 1 fails. In view of the claims that depend from claim 1, 18, or 32, we cannot sustain the § 102 rejection of claims 1-9, 18-25, 32-38, 43, 44, 47, 48, 51, and 52.

Section 102 -- Claims 10-14, 16, 17, 26-29, 31, 39-42, 45, 46, 49, 50

Each of independent claims 10, 26, and 39 recites performing type checking to determine whether a selected method or property of a first hardware device class is valid for a second hardware device class. The

rejection contends that Teranishi discloses the claimed "type checking" in column 5, lines 6 through 23.

However, we agree with Appellants that the indicated section of Teranishi fails to disclose type checking as claimed. Moreover, the text appears to describe disadvantages of the prior art with respect to Teranishi, as opposed to Teranishi's contribution to the art (which the rejection relies on in alleging disclosure of other claim limitations in the § 102 rejection of each of independent claims 10, 26, and 39).

In view of the claims that depend from claim 10, 26, or 39, we cannot sustain the § 102 rejection of claims 10-14, 16, 17, 26-29, 31, 39-42, 45, 46, 49, and 50.

Section 103 -- Claims 15 and 30

Because claim 15 depends from claim 10 and claim 30 depends from claim 26, and the addition of McKaskle does not remedy the deficiencies in the rejection applied against the base claims, we cannot sustain the § 103(a) rejection of claims 15 and 30 over Teranishi and McKaskle.

DECISION

We reverse the rejection of claims 1-14, 16-29, and 31-52 under 35 U.S.C. § 102(e) as being anticipated by Teranishi.

We reverse the rejection of claims 15 and 30 under 35 U.S.C. § 103(a) as being unpatentable over Teranishi and McKaskle.

REVERSED

msc

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